

What is claimed is:

- 1 1. A semiconductor device, comprising:
 - 2 a semiconductor substrate;
 - 3 a first metal layer formed overlying the semiconductor
 - 4 substrate;
 - 5 an etch stop layer formed overlying the first metal
 - 6 layer and the semiconductor substrate;
 - 7 a dielectric layer formed overlying the etch stop
 - 8 layer; and
 - 9 a second metal layer penetrating the dielectric layer
 - 10 and the etch stop layer and electrically
 - 11 connected to the first metal layer;
 - 12 wherein, the etch stop layer has a dielectric constant
 - 13 smaller than 3.5; and
 - 14 wherein, the dielectric layer has a dielectric constant
 - 15 smaller than 3.0.
- 1 2. The semiconductor device of claim 1, wherein the
- 2 etch stop layer has a compressive stress of $0\sim 1 \times 10^9$
- 3 dynes/cm².

1 3. The semiconductor device of claim 2, wherein the
2 dielectric layer has a tensile stress approximating to the
3 compressive stress of the etch stop layer.

1 4. The semiconductor device of claim 1, wherein the
2 dielectric layer has a film hardness greater than 0.2GPa and
3 an elastic modulus greater than 5GPa.

1 5. The semiconductor device of claim 1, wherein the
2 etch stop layer is an oxygen-doped silicon carbide (SiOC)
3 layer, and the dielectric layer is a porous organo-silicate
4 glass (OSG) layer.

1 6. The semiconductor device of claim 1, wherein each
2 of the first metal layer and the second metal layer is a
3 copper layer.

1 7. The semiconductor device of claim 1, wherein the
2 etch stop layer is a composite film comprising a first etch
3 stop layer and a second etch stop layer, in which the first
4 etch stop layer is formed overlying the second etch stop
5 layer.

1 8. The semiconductor device of claim 7, wherein a
2 first etching selectivity S_1 of the first etch stop layer to
3 the dielectric layer, and a second etching selectivity S_2 of
4 the second etch stop layer to the dielectric layer satisfy
5 the formula: $S_1 \neq S_2$.

1 9. The semiconductor device of claim 8, wherein S_1
2 and S_2 satisfy the formula: $0 < S_1 < S_2$.

1 10. The semiconductor device of claim 7, wherein a
2 first thickness T_1 of the first etch stop layer and a second
3 thickness T_2 of the second etch stop layer satisfy the
4 formula: $T_2 < (T_1 + T_2) / 3$.

1 11. The semiconductor device of claim 7, wherein the
2 etch stop layer is a SiCO-based composite deposition.

1 12. The semiconductor device of claim 11, wherein the
2 first etch stop layer is a SiC film and the second etch stop
3 layer is a SiO film.

1 13. The semiconductor device of claim 7, wherein each
2 of the first etch stop layer and the second etch stop layer

3 is SiCN, SiCO, SiN, SION, SiC, or SiO, or a combination
4 thereof.

1 14. A copper damascene structure, comprising:
2 a semiconductor substrate;
3 a first copper layer formed overlying the semiconductor
4 substrate;
5 an etch stop layer formed overlying the first copper
6 layer and the semiconductor substrate;
7 a dielectric layer formed overlying the etch stop
8 layer, in which a damascene opening is formed to
9 penetrate the dielectric layer and the etch stop
10 layer to expose the first copper layer; and
11 a second copper layer formed in the damascene opening
12 and electrically connected to the first copper
13 layer;
14 wherein, the etch stop layer has a dielectric constant
15 smaller than 3.5; and
16 wherein, the dielectric layer has a dielectric constant
17 smaller than 3.0.

1 15. The copper damascene structure of claim 14,
2 wherein the etch stop layer has a dielectric constant of
3 1.0~3.5, and the dielectric layer has a dielectric constant
4 of 1.0~3.0.

1 16. The copper damascene structure of claim 14,
2 wherein the etch stop layer has a compressive stress of
3 $0\sim 1 \times 10^9$ dynes/cm².

1 17. The copper damascene structure of claim 16,
2 wherein the dielectric layer has a tensile stress
3 approximating to the compressive stress of the etch stop
4 layer.

1 18. The copper damascene structure of claim 14,
2 wherein the dielectric layer has a film hardness greater
3 than 0.2GPa and an elastic modulus greater than 5GPa.

1 19. The copper damascene structure of claim 14,
2 wherein the etch stop layer is an oxygen-doped silicon
3 carbide (SiOC) layer, and the dielectric layer is a porous
4 organo-silicate glass (OSG) layer.

1 20. The copper damascene structure of claim 14,
2 wherein the second copper layer is a copper single damascene
3 structure or a copper dual damascene structure.

1 21. The copper damascene structure of claim 14,
2 wherein the etch stop layer is a composite film comprising a
3 first etch stop layer and a second etch stop layer, in which
4 the first etch stop layer is formed overlying the second
5 etch stop layer.

1 22. The copper damascene structure of claim 21,
2 wherein a first etching selectivity S_1 of the first etch
3 stop layer to the dielectric layer, and a second etching
4 selectivity S_2 of the second etch stop layer to the
5 dielectric layer, satisfy the formula: $S_1 \neq S_2$.

1 23. The copper damascene structure of claim 22,
2 wherein at least one of S_1 and S_2 is larger than zero.

1 24. The copper damascene structure of claim 22,
2 wherein S_1 and S_2 satisfy the formula: $0 < S_1 < S_2$.

1 25. The copper damascene structure of claim 21,
2 wherein a first thickness T_1 of the first etch stop layer
3 and a second thickness T_2 of the second etch stop layer
4 satisfy the formula: $T_2 < (T_1 + T_2)/3$.

1 26. The copper damascene structure of claim 21,
2 wherein the etch stop layer is a SiCO-based composite
3 deposition.

1 27. The copper damascene structure of claim 26,
2 wherein the first etch stop layer is a SiC film, and the
3 second etch stop layer is a SiO film.

1 28. The copper damascene structure of claim 21,
2 wherein each of the first etch stop layer and the second
3 etch stop layer is SiCN, SiCO, SiN, SiON, SiC, or SiO, or a
4 combination thereof.

1 29. A fabrication method for a semiconductor device,
2 comprising the steps of:

3 providing a semiconductor substrate having a first
4 metal layer;

5 forming an etch stop layer overlying the first metal
6 layer and the semiconductor substrate, wherein
7 the etch stop layer has a dielectric constant
8 smaller than 3.5;
9 forming a dielectric layer overlying the etch stop
10 layer, wherein the dielectric layer has a
11 dielectric constant smaller than 3.0;
12 forming an opening which penetrates the dielectric
13 layer and the etch stop layer and exposes the
14 first metal layer; and
15 forming a second metal layer in the opening, in which
16 the second metal layer is electrically connected
17 to the first metal layer.

1 30. The fabrication method for a semiconductor device
2 of claim 29, wherein the etch stop layer has a compressive
3 stress of $0\sim 1 \times 10^9$ dynes/cm², and the dielectric layer has a
4 tensile stress approximating to the compressive stress of
5 the etch stop layer.

1 31. The fabrication method for a semiconductor device
2 of claim 29, wherein the dielectric layer has a film
3 hardness greater than 0.2GPa and an elastic modulus greater
4 than 5GPa.

1 32. The fabrication method for a semiconductor device
2 of claim 29, wherein the etch stop layer is an oxygen-doped
3 silicon carbide (SiOC) layer, and the dielectric layer is a
4 porous organo-silicate glass (OSG) layer.

1 33. The fabrication method for a semiconductor device
2 of claim 29, wherein the opening filled with the second
3 metal layer is a copper damascene structure.

1 34. The fabrication method for a semiconductor device
2 of claim 29, wherein the etch stop layer is a composite film
3 comprising a first etch stop layer and a second etch stop
4 layer, in which the first etch stop layer is formed
5 overlying the second etch stop layer.

1 35. The fabrication method for a semiconductor device
2 of claim 34, wherein a first etching selectivity S_1 of the

3 first etch stop layer to the dielectric layer, and a second
4 etching selectivity S_2 of the second etch stop layer to the
5 dielectric layer satisfy the formula: $S_1 \neq S_2$.

1 36. The fabrication method for a semiconductor device
2 of claim 35, wherein S_1 and S_2 satisfy the formula: $0 < S_1 < S_2$.

1 37. The fabrication method for a semiconductor device
2 of claim 34, wherein a first thickness T_1 of the first etch
3 stop layer and a second thickness T_2 of the second etch stop
4 layer satisfy the formula: $T_2 < (T_1 + T_2)/3$.

1 38. The fabrication method for a semiconductor device
2 of claim 34, wherein the etch stop layer is a SiCO-based
3 composite deposition.

1 39. The fabrication method for a semiconductor device
2 of claim 38, wherein the first etch stop layer is a SiC
3 film, and the second etch stop layer is a SiO film.

1 40. The fabrication method for a semiconductor device
2 of claim 34, wherein each of the first etch stop layer and

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3 the second etch stop layer is SiCN, SiCO, SiN, SiON, SiC, or
4 SiO, or a combination thereof.